IN THE SPECIFICATION:

Please amend the second full paragraph on page 2 as follows:

State of the Art: Integrated circuits (ICs) contain numerous individual devices, such as transistors and capacitors, that are interconnected by an intricate network of horizontal and vertical conductive lines commonly termed ~~interconnects.~~ "interconnects." Exemplary interconnect structures are disclosed in U.S. Patent Nos. 5,545,590, 5,529,954, 5,300,813, 4,988,423, and 5,356,659, each of which patents is hereby incorporated herein by reference.

Please amend the third full paragraph on page 2 as follows:

Aluminum interconnect structures are decreasing in size and pitch (spacing), as the industry trend continues ~~to, and including,~~ toward, and includes submicron features and pitches. The resultant reduction in structure sizes leads to numerous reliability concerns, including electromigration and stress voiding of the interconnect structures.

Please amend the paragraph bridging pages 3 and 4 as follows:

Several methods have been proposed to reduce stress notching. One proposed method uses a material less susceptible to stress notching, such as copper (Cu) or tungsten (W), in the conductive line. Using Cu in conductive lines, however, has in the past resulted in several problems. First, copper is difficult to etch. Second, adhesion between copper and adjacent insulating layers is poor and thus poses reliability concerns. Third, adding Cu to Al lines may reduce stress notching, but beyond a certain Cu concentration, device performance may begin to degrade. Fourth, as conductive line geometries shrink, adding Cu to Al lines seems less effective in reducing stress notching. Finally, even using Cu interconnects in the manner employed in the prior art can still lead to notching effects, especially at 0.1 μm geometries and below since, at such dimensions, line widths have become so small that any imperfection can cause ~~opens.~~ openings. Using W in Al conducting lines is also undesirable — W has a high resistivity and, therefore, reduces signal speed.

Please amend the third full paragraph on page 4 as follows:

U.S. Patent No. 5,317,185, incorporated herein by reference, describes still another proposed method for reducing stress notching. This patent discloses an IC device having a plurality of conductive lines where the outermost conductive line is a stress-reducing line. This stress-reducing line is a non-active structure ~~which~~ that reduces stress concentrations in the inner conductive lines.

Please amend the first full paragraph on page 5 as follows:

The present invention also relates to a metallization structure comprising a substrate having a metal layer disposed thereon, a dielectric layer having an aperture therethrough disposed on the substrate so the bottom of the aperture exposes the upper surface of the metal layer, at least one metal spacer on the sidewall of the aperture, and a conducting layer filling the remaining portion of the aperture. The metal layer and metal spacer preferably ~~comprises~~ comprise titanium, such as Ti or TiN. At least one upper metal layer may be disposed on the conducting layer.

Please amend the first full paragraph on page 6 as follows:

The present invention provides several advantages when compared to the prior art. One advantage is that ~~thermally induced~~ thermally induced stress voids are reduced because the metal layer and metal spacer comprise materials exhibiting good thermal-voiding avoidance characteristics. Another advantage is that the size of conductive lines can be shrunk further in comparison to dimensions achievable by conventional processes, since only one additional deposition and etch step, without an additional masking step, is needed to form the metallization structure. Shrinking of conductive lines is necessary as device geometries decrease to less than 0.1 μm. At these small geometries, even small notches can significantly decrease conductivity.

Please amend the third full paragraph on page 7 as follows:

Generally, the present invention relates to a metallization structure for interconnects and semiconductor devices including same. Specifically, the present invention reduces stress voiding, especially ~~thermally-induced~~ thermally induced stress voiding, in conducting lines. The metallization structures described below exemplify the present invention without reference to a specific device because the inventive process and structure can be modified by one of ordinary skill in the art for any desired device.

Please amend the paragraph bridging pages 7 and 8 as follows:

One embodiment of a process and resulting metallization structure of the present invention is illustrated in Figures 1, 2, 3a, and 3b. This embodiment may be characterized as a predominantly "subtractive" process, in comparison to the second embodiment discussed hereinafter, in that portions of superimposed material layers are removed to define the interconnect structure features, such as lines. As shown in Figure 1, a portion of semiconductor device 2 includes substrate 4 with overlying first dielectric layer 6. Substrate 4 may be any surface suitable for integrated circuit device formation, such as a silicon or other semiconductor wafer or other substrate, and may be doped and/or include an epitaxial layer. Substrate 4 may also be an intermediate layer in a semiconductor device, such as a metal contact layer or an interlevel dielectric layer. Preferably, substrate 4 is a silicon wafer or bulk silicon region, such as a ~~silicon-on-insulator~~ silicon-on-insulator (SOI) or silicon-on-sapphire (SOS) structure.

Please amend the second full paragraph on page 8 as follows:

Overlying first dielectric layer 6 is metal layer 8. One or more individual metal layers may be used as metal layer 8. For example, if two superimposed metal layers are employed (represented by the dashed line in metal layer 8), an adhesion-promoting metal layer can be a first, lower portion of metal layer 8 on first dielectric layer 6 and a ~~stress-reducing~~ stress-reducing layer can be a second, upper portion of metal layer 8. Other metal layers might be included for other functions, such as a layer for reducing electromigration. Preferably, a

single metal layer is used as metal layer 8, especially when the single layer can reduce electromigration, function as an ~~adhesion promoting~~ adhesion-promoting layer, and function as a ~~stress reducing~~ stress-reducing layer. If two metal layers are employed, the first, upper metal layer may, for example, comprise tantalum, titanium, tungsten, TaN, or TiN and the second, lower metal layer overlying first dielectric layer 6 may, for example, comprise TiN, TiW, WN, or TaN.

Please amend the paragraph bridging pages 9 and 10 as follows:

Conducting layer 10 is then formed over metal layer 8. Conducting layer 10 may comprise any conducting material used in IC device fabrication. Preferably, conducting layer 10 comprises a conducting metal, such as Al, optionally containing other elements such as Si, W, Ti, and/or Cu. More preferably, conducting layer 10 is an ~~aluminum-copper~~ aluminum-copper alloy. Conducting layer 10 may also be formed of Cu. Conducting layer 10 may be formed by any method used in IC device fabrication such as CVD or PVD techniques. Preferably, conducting layer 10 is deposited by a PVD method such as sputtering, as known in the art. Second dielectric layer 12 is next deposited or otherwise formed on top of conducting layer 10. Second dielectric layer 12 comprises any dielectric material used in IC device fabrication, including those listed above. Preferably, second dielectric layer 12 comprises a material that serves as an etch stop, as explained below. More preferably, second dielectric layer 12 comprises fluorine-doped silicon oxide or other low dielectric constant material. Second dielectric layer 12 may be formed by any suitable process giving the desired physical and chemical characteristics, such as CVD, PECVD (plasma enhanced chemical vapor deposition), spin-on methods, or otherwise, depending upon the dielectric material selected. For use of the preferred fluorine-doped silicon oxide, the preferred deposition method is PECVD.

Please amend the second full paragraph on page 10 as follows:

As also shown in Figure 2, second metal layer 14 (also termed a metal spacer layer) is then deposited on first dielectric layer 6 and over multi-layer structure 13. In similar fashion to the structure of metal layer 8, one or more individual metal layers, illustrated by the dashed line within second metal layer 14, may be used as second metal layer 14. Preferably, a single metal layer is used as second metal layer 14 for the same reasons as those set forth for metal layer 8.

Please amend the third full paragraph on page 10 as follows:

Like metal layer 8, second metal layer 14 includes not only ~~metals,~~ metals but their alloys and compounds (e.g., nitrides and silicides). Preferably, when conducting layer 10 comprises ~~aluminum ,~~ aluminum, second metal layer 14 comprises Ti. If conducting layer 10 comprises Cu, second metal layer 14 preferably comprises TiW. More preferably, second metal layer 14 comprises the same metal as ~~first~~ metal layer 8. ~~Metal~~ Second metal layer 14 may be deposited or otherwise formed by a process similar to the process used to form metal layer 8. Preferably, second metal layer 14 is formed by a conformal deposition process, such as CVD.

Please amend the paragraph bridging pages 10 and 11 as follows:

Next, as illustrated in Figure 3a, second metal layer 14 is spacer etched to remove portions of the second metal layer 14 on first dielectric layer 6 and on second dielectric layer 12, thereby leaving metal spacers 16 on the multi-layer structure 13. A spacer etch is a directional sputtering etch ~~which~~ that removes second metal layer 14 so that metal spacers 16 remain on the sidewalls of multi-layer structure 13. The spacer etch uses the first and second dielectric layers as an etch stop.

Please amend the first full paragraph on page 11 as follows:

If desired, second dielectric layer 12 can then be removed. Second dielectric layer 12 can be removed by any process ~~which~~ that removes the second dielectric layer without removing first dielectric layer 6. If the first and second dielectric layers comprise different materials (e.g.,

when second dielectric layer 12 is silicon oxide and the first dielectric layer 6 is BPSG), any process ~~which~~ that selectively etches the second dielectric layer 12 can be employed. The etch process would also remove the portions of metal spacers 16 laterally adjacent second dielectric layer 12, thus resulting in the metallization structure illustrated in Figure 3b. When the first and second dielectric layers 6, 12 are similar or have similar etch rates (e.g., when both are silicon oxide or fluorine-doped), a facet etch process can be used. As shown in broken lines in Figure 3b, when the first and second dielectric layers 6 and 12 exhibit similar etch rates, the thickness of first dielectric layer 6 will be reduced by substantially the thickness of removed second dielectric layer 12.

Please amend the second full paragraph on page 11 as follows:

The metallization structures illustrated in Figures 3a and 3b reduce ~~thermally induced~~ thermally induced stress voids in conductive lines 100. Metal layer 8 and metal spacers 16 serve as a protective coating at the respective lower and lateral surfaces of conductive lines 100 and at intersections thereof, thereby reducing the incidence of stress voids by preventing them from starting at these surfaces and intersections thereof on conductive line 100. Metal layer 8 and metal spacers 16 also increase reliability of conductive line 100 without reducing its resistance.

Please amend the paragraph bridging pages 11 and 12 as follows:

Another embodiment of a process and resulting metallization structures of the present invention is represented in Figures 4 through 11. This embodiment may be characterized as more of an "additive" method or process than that described with respect to Figures 1 through ~~3, in~~ 3b, in that metallization structures for interconnects are formed by deposition in apertures, such as vias or trenches. As such, it should be noted that cusping of material deposited to line the sidewall or sidewalls of an aperture may be of concern if the method of deposition is not sufficiently anisotropic or, in some instances, the aperture exhibits a very high aspect ratio. In Figure 4, metal layer 52 has been deposited or otherwise formed over substrate 50. Any of the substrates employable as substrate 4 above can be used as substrate 50. Preferably, substrate 50

is a silicon wafer or bulk silicon region, such as an SOI or SOS structure. Such substrate 50 can have active and passive devices and other electrical circuitry fabricated on it, these circuit structures being interconnected by the metallization structures of the present invention. Therefore, a direct electrical path may exist between the devices and circuitry of the substrate 50 (or 4), the devices and circuitry being omitted herein for simplicity.

Please amend the first full paragraph on page 12 as follows:

Metal layer 52 may comprise a discrete conductive member, such as a wire, a stud, or a contact. Preferably, metal layer 52 is substantially similar to metal layer 8 described above and may be of any of the same metals, alloys or compounds. If desired, a dielectric layer 51 can be formed on substrate 50 and beneath metal layer 52. Dielectric layer 51 is substantially similar to first dielectric layer 6 described above.

Please amend the second full paragraph on page 12 as follows:

As illustrated in Figure 4, dielectric layer 54 is then deposited or otherwise formed on metal layer 52. Dielectric layer 54 may be any dielectric or insulating material used in IC device fabrication, such as those listed above for second dielectric layer 12. Preferably, dielectric layer 54 is silicon oxide or spin-on glass (SOG). Dielectric layer 54 may be formed by any IC device fabrication process giving the desired physical and chemical characteristics.

Please amend the third full paragraph on page 12 as follows:

An aperture 56 such as a via or trench ~~56 is~~ is then formed in dielectric layer 54 by removing a portion of dielectric layer 54 to expose underlying metal layer 52. Aperture 56 may be formed by any IC device manufacturing method, such as a photolithographic patterning and etching process.

Please amend the paragraph bridging pages 12 and 13 as follows:

As shown in Figure 5, metal collar 60 is formed on the sidewalls of aperture 56, using a spacer etch as known in the art. It will be understood that the term "collar" encompasses a co-parallel spacer structure 60 if aperture 56 is a trench extending over substrate 50. Similar to second metal layer 14, collar 60 may contain one or more metal layers with a single metal layer preferably used. Also in similar fashion to second metal layer 14, collar 60 may include not only metals, but their alloys and compounds. Like second metal layer 14, any metal can be employed in collar 60, provided it exhibits the desired characteristics, either alone or when combined with other metal layers, and the metals applicable to second metal layer 14 are equally applicable to collar 60. Preferably, collar 60 comprises the same metal as metal layer 52. More preferably, when metal layer 52 comprises Al, collar 60 comprises Ti.

Please amend the first full paragraph on page 13 as follows:

Collar 60 is formed by an IC device fabrication process ~~which~~ that does not degrade metal layer 52, yet forms a collar or spacer-like ~~structures~~ structure 60 on the sidewall or sidewalls of aperture 56. For example, layer 61 (shown in Figure 4) of a material from which collar 60 is formed can be conformally deposited on dielectric layer 54 and the walls of aperture 56. Conformal coverage yields a substantially vertical sidewall in the dielectric aperture. While not preferred, a partially conformal layer of the material can be deposited instead. A highly conformal process is preferably employed to form layer 61. Portions of layer 61 on the bottom of aperture 56 and top of dielectric layer 54 are then removed, preferably by using an appropriate directional etch, such as reactive ion etching (RIE).

Please amend the second full paragraph on page 13 as follows:

Conducting layer 62 is next deposited or otherwise formed to fill aperture 56 and extend over dielectric layer 54, as shown in broken lines in Figure 5. Conducting layer 62 may be deposited by any IC device fabrication method yielding the desired characteristics. For example, conducting layer 62 may be deposited by a conformal or non-conformal deposition process. An

abrasive planarization process, such as ~~chemical-mechanical~~ chemical-mechanical planarization (CMP), is then used to remove portions above the horizontal plane of the upper surface of dielectric layer 54 and leave conductive plug (in a ~~via 56)~~ via) or line (in a ~~trench 56)~~ trench) 64 as illustrated in Figure 6.

Please amend the first full paragraph on page 14 as follows:

Dielectric layer 54 can then be optionally removed, thus forming the interconnect structure represented in Figure 7a. Dielectric layer 54 can be removed by any process ~~which~~ that does not degrade any of metal layer 52, conducting layer 62, or collar 60. For example, when dielectric layer 54 is silicon oxide, it may be removed by an HF wet etch solution or an oxide dry etch process. If desired, portions of metal layer 52 can then be removed, preferably by a directional etching process, to obtain the interconnect structure shown in Figure 7b.

Please amend the third full paragraph on page 14 as follows:

Upper metal layer 66 can be formed over conductive plug 64 in the following manner. Conducting layer 62 is deposited in aperture 56 and over dielectric layer 54 as described above with respect to Figure 5. Prior to completely filling aperture 56, however, the deposition of conducting layer 62 is halted as shown at 62a in Figure 5, leaving an upper portion of aperture 56 empty ~~(i.e.,~~ (i.e., a recess is left at the top of aperture 56). Upper metal layer 66 is then deposited over conducting layer 62, including the still-empty upper portion of aperture 56. Portions of conducting layer 62 and upper metal layer 66 above the horizontal plane of dielectric layer 54 are then removed by a planarization process, such as CMP, to form a completely enveloped, or clad, interconnect structure. If desired, portions of dielectric layer 54 and metal layer 52 flanking the interconnect structure can be removed as described above to form the structure of Figure 9.

Please amend the first full paragraph on page 15 as follows:

In another process variant, after forming metal layer 52 on substrate 50 and forming dielectric layer 54 with aperture 56 therethrough, but prior to forming collar 60, conductive plug

or line 64 could be formed in aperture 56 as described above. Upper metal layer 66 could then be deposited, as described above, over conductive plug or line 64 and dielectric layer 54 to obtain the structure illustrated in Figure 10. Portions of upper metal layer 66 not overlying conductive plug or line 64 could then be removed by a photolithographic pattern and etch process, followed by removing dielectric layer 54 by the method described above, to obtain the structure illustrated in Figure 11. As explained above, the structure of Figure 11 could then have a conformed metal layer deposited and etched (similar to the deposition and etch of second metal layer 14 above) to form a structure similar to that depicted in Figure 3a.